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S/N 09/785,006 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Aaron M. Schoenfeld	Examiner:	Evan P. Pert
Serial No.:	09/785,006	Group Art Unit:	2813
Filed:	February 16, 2001	Docket:	303.259US3
Title:	GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS		

7/13/01

RESPONSE TO RESTRICTION REQUIREMENT AND AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

In response to the Restriction Requirement mailed June 8, 2001, Applicant elects, without traverse, Group I (claims 11-25). Applicant respectfully cancels remaining claims 26-34 (Group II) without prejudice, reserving the right to reintroduce their subject matter them in a divisional application at a later date.

IN THE CLAIMS

Please add new claims 35-43:

35. (New) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar edges, where the planar edges are substantially transverse to the first planar surface and the second planar surface.

36. (New) The semiconductor die as recited in claim 35, wherein each planar edge has an entirely flat, smooth surface.

37. (New) The semiconductor die as recited in claim 35, wherein the semiconductor die has a substantially rectangular shape.